

System Architecture Specification: Master & Slave BMS

Communication Topology

Overview

The Gigavolt Battery Management System architecture utilizes a two-tier hierarchical distributed processing model consisting of one Master BMS Controller (**BMS-MST-GEN2**) and up to 24 modular Slave Balancing Boards (**BMS-CAS-LFP** for LFP platforms or **BMS-CAS-NMC** for NMC platforms).

Physical Layer & Wiring Specification

- **Topology:** Linear daisy-chain bus utilizing shielded twisted-pair (STP) cabling (Part Number: **HAR-CAN-35**).
- **Characteristic Impedance:** 120 Ω nominal.
- **Termination:** 120 Ω metal film terminating resistors installed at physical node 0 (Master) and physical node 24 (terminal slave). Total bus resistance measured across CAN-H and CAN-L with control power removed must read exactly 60 $\Omega \pm 2 \Omega$.
- **Galvanic Isolation:** Optical isolation barrier rated for 2,500 V RMS continuous between low-voltage digital processing circuitry and high-voltage battery cell sense lines.

Frame Protocol & Sampling Timing

- **BMS Telemetry Sampling Frequency:** 100 ms loop.
- **Cell Voltage Measurement Resolution:** 14-bit ADC providing ± 1.0 mV resolution across the 0.00 V to 5.00 V operating window.
- **Temperature Sensor Inputs:** 4 precision 10k NTC thermistors per module cassette.
- **Fault Reporting Thresholds:**
 - If CAN heartbeat packet is missing for > 3 consecutive cycles (300 ms), the Master BMS trips error code **ERR_BMS_301** (Module Communication Lost) and commands immediate inverter ramping down to 0 kW.
 - If any individual cell drops below 2.00 V while under discharge, slave triggers emergency interrupt flag within 5 ms, escalating to **ERR_VOLT_102**.

